Amendments to the Specification:

Replace the paragraph on page 17, line 15 to page 18, line 7 with the following amended paragraph:

The SPI driver ~~225~~ 212 implements initialization of the SPI unit 24 (slave mode setting and "Disabled" setting after the end of SPI transmission) and start of transmission/reception for enabling the SPI unit in response to a request from a communication client just before transmission of a command message. Further, to detect a garbled message in transmission/reception, the SPI driver ~~225~~ 212 calculates a checksum of the transmit buffer 24B in the SPI unit 24 before transmission, writes the checksum and the 1's complement of the checksum in the command message, calculates a checksum of the receive buffer 24A of the SPI unit 24 after reception, and checks whether the checksum and the 1's complement are right. In this embodiment, however, "Inhibiting an interrupt ("Disabled") after the end of SPI transmission" is set in the initialization processing to inform the end of the SPI transmission by a response message. To generate an interrupt at the end of an SPI transmission instead of a response message, "Enabled" should be set in the initialization processing.

Replace the paragraph on page 20, line 12 to page 21, line 2 with the following amended paragraph:

The SPI driver ~~325~~313 implements initialization of the SPI unit 34 (master mode setting and "Enable" setting after the end of an SPI transmission) and transmission/reception starting processing which starts an SPI transmission in response to an instruction from the communication server group 324. In the transmission/reception starting processing, the SPI driver ~~325~~313 starts an SPI transmission by means of a register of the SPI unit 34. In the SPI transmission, the

SPI unit 34 keeps on generating a CLK signal, transfers data from the transmit buffer 34B to the receive buffer 24A of the SPI unit 24 in the control processor 2 in synchronism with the CLK and data from the transmit buffer 24B of the SPI unit 24 in the control processor 2 to the receive buffer 34A. In response to an interrupt after the SPI transmission ends, the SPI driver ~~325~~313 causes the communication manager 323 to call a communication server which started the communication manager 323.